What is claimed is:

1. A method which generates an IC tester control consisting of numerous test instructions for a plurality of specific test environments, which can generate and measure analog and digital signals for an IC, in particular a mixed-signal IC,
wherein
the method obtains data and control instructions from multidimensional test matrices independent of the test environment, such as matrix-like databases or libraries,
the data and control instructions independent of the test environment are converted by means of a code generator into a syntax which is dependent on the test environment and which can be integrated into a general syntax dependent on the test environment, so that the syntax dependent on the test environment and the general syntax dependent on the test environment together form a complete control, comprising analog and digital signals, for one of the specific test environments.

2. The method as claimed in claim 1, wherein, during its conversion phase, the code generator employs a library group in which are integrated various libraries which contain at least partial information with respect to
a) the test environment,
b) the syntax dependent on the test environment,
c) the test environment resources,
d) the sequence of test methods,
e) the standard functions of the test environment,

f) the load board structure,

g) the standard functions dependent on the load board and

h) the code generator optimization.

3. The method as claimed in claim 1, wherein a multidimensional test matrix has,
in a first dimension, data on the number and arrangement of pins of the IC,
in a further dimension, data on the meaning, the name and the signal flow direction of the pins of the IC,
in a further dimension, sequences of test instructions,
in a further dimension, test instruction headings which summarize individual test instructions,
in one dimension, specifies general test conditions,
in one dimension, specifies the start conditions for a test,
in one dimension, specifies test patterns,
in one dimension, specifies functional descriptions of the tests,
in one dimension, specifies switching values,
in one dimension, specifies conditions for quality sorting of ICs.

4. The method as claimed in claim 1, wherein the code generator comprises at least one of the following components;
- a DC test generator which reads out and converts the data and control instructions from matrices, which generate DC voltage values for an

IC in the test environment,

- an AC test generator which reads out and converts the data and control instructions from matrices, which generate AC voltage values or signal curves for an IC in the test environment,
- a digital test generator which reads out and converts the data and control instructions from matrices, which generate digital voltage values for an IC in the test environment,
- a load board generator which reads out and converts the data and control instructions from matrices, which refer to the resources and requirements with respect to the load conditions of the load boards of the test environment,
- a test rule verifier which checks whether the data and control instructions of the syntax dependent on the test environment can be executed in the test environment,

and the code generator runs through a multistage method

- in the first stage of which the data and control instructions of a matrix are made available to the code generator as source information,
- in the second stage of which the source information is processed in succession, in each case by one of the components, the last component being the test rule verifier,
- and, in the third stage of which, the converted data and control instructions are modified by means of an optimizer with respect to resource utilization of the test environment, test speed, test sequences or waiting and idle times between

individual data and control instructions.

5. The method as claimed in claim 1, wherein a processible data sheet of the IC serves as the origin for the matrices independent of the test environment, on the basis of which data sheet automated test description documentations are generated from the matrices and name, in a generally legible manner, the scope, the type, the duration and the type of the data and control instructions.

6. The method as claimed in claim 1, wherein signals which are analog and/or digital are read in from the test environment, preferably with a time lag after superposition of signals of the control, in order to be evaluated via mixed-signal test methods, such as, for example, a method for the gain or gains, the voltage ratios, the frequency responses, the phase positions, the wave shapes, the harmonics and/or the transit-time behavior.

7. A method which generates an IC tester control, consisting of numerous test instructions, for a plurality of specific test environments, which can generate and measure analog and digital signals for an IC, in particular a mixed-signal IC,
wherein
the individual specific test environments differ from one another in their structure and/or their syntax,
the method obtains data and control instructions from multidimensional test matrices independent of

the test environment, such as matrix-like databases or libraries,
the data and control instructions independent of the tester environment are converted by means of a code generator into a syntax which is dependent on the test environment and which can be integrated into a general syntax dependent on the test environment, so that the syntax dependent on the test environment and the general syntax dependent on the test environment together form a complete control, comprising analog and digital signals, for one of the specific test environments.

8. The method as claimed in claim 7, wherein, in the multidimensional test matrices, it is possible to list test methods which enable both digital and analog signals of the control of the test environment to occur synchronously.

9. The method as claimed in claim 8, wherein a multidimensional test matrix has,
in a first dimension, data on the number and arrangement of pins of the IC,
in a further dimension, data on the meaning, the name and the signal flow direction of the pins of the IC,
in a further dimension, sequences of test instructions,
in a further dimension, test instruction headings which summarize individual test instructions,
in one dimension, specifies general test conditions,
in one dimension, specifies the start conditions

for a test,
in one dimension, specifies test patterns,
in one dimension, specifies functional descriptions of the tests,
in one dimension, specifies switching values,
in one dimension, specifies conditions for quality sorting of ICs.

10. The method as claimed in claim 9, wherein, during its conversion phase, the code generator employs a library group in which are integrated various libraries which contain at least partial information with respect to
a) the test environment,
b) the syntax dependent on the test environment,
c) the test environment resources,
d) the sequence of test methods,
e) the standard functions of the test environment,
f) the load board structure,
g) the standard functions dependent on the load board and
h) the code generator optimization.

11. The method as claimed in claim 7, wherein furthermore the code generator comprises at least one of the following components;
- a DC test generator which reads out and converts the data and control instructions from matrices, which generate DC voltage values for an IC in the test environment,
- an AC test generator which reads out and converts the data and control instructions from matrices, which generate AC voltage values or

signal curves for an IC in the test environment,

- a digital test generator which reads out and converts the data and control instructions from matrices, which generate digital voltage values for an IC in the test environment,

- a load board generator which reads out and converts the data and control instructions from matrices, which refer to the resources and requirements with respect to the load conditions of the load boards of the test environment,

- a test rule verifier which checks whether the data and control instructions of the syntax dependent on the test environment can be executed in the test environment,

and the code generator runs through a multistage method

- in the first stage of which the data and control instructions of a matrix are made available to the code generator as source information,

- in the second stage of which the source information is processed in succession, in each case by one of the components, the last component being the test rule verifier,

- and, in the third stage of which, the converted data and control instructions are modified by means of an optimizer with respect to resource utilization of the test environment, test speed, test sequences or waiting and idle times between individual data and control instructions.

12. The method as claimed in claim 10, wherein a processible data sheet of the IC serves as the

origin for the matrices independent of the test environment, on the basis of which data sheet automated test description documentations are generated from the matrices and name, in a generally legible manner, the scope, the type, the duration and the type of the data and control instructions.

13. The method as claimed in claim 8, wherein signals which are analog and/or digital are read in from the test environment, preferably with a time lag after superposition of signals of the control, in order to be evaluated via mixed-signal test methods, such as, for example, a method for the gain or gains, the voltage ratios, the frequency responses, the phase positions, the wave shapes, the harmonics and/or the transit-time behavior.

14. A method which generates an IC tester control, consisting of numerous test instructions, for a plurality of specific test environments, which can generate and measure analog and digital signals for an IC, in particular a mixed-signal IC,
wherein
the method obtains data and control instructions from multidimensional test matrices independent of the test environment, such as matrix-like databases or libraries,
the data and control instructions independent of the test environment are converted by means of a code generator into a syntax which is dependent on the test environment and which can be integrated into a general syntax dependent on the test

environment, so that the syntax dependent on the test environment and the general syntax dependent on the test environment together form a complete control, comprising analog and digital signals, for one of the specific test environments, and test methods which allow both digital and analog signals of the control of the test environment to occur synchronously can be listed in the multidimensional test matrices.

15. The method as claimed in claim 14, wherein, during its conversion phase, the code generator employs a library group in which are integrated various libraries which contain at least partial information with respect to

a) the test environment,
b) the syntax dependent on the test environment,
c) the test environment resources,
d) the sequence of test methods,
e) the standard functions of the test environment,
f) the load board structure,
g) the standard functions dependent on the load board and
h) the code generator optimization.

16. The method as claimed in claim 15, wherein signals which are analog and/or digital are read in from the test environment, preferably with a time lag after superposition of signals of the control, in order to be evaluated via mixed-signal test methods, such as, for example, a method for the gain or gains, the voltage ratios, the frequency responses, the phase positions, the wave shapes,

the harmonics and/or the transit-time behavior.

17. The method as claimed in claim 16, wherein a multidimensional test matrix has,
in a first dimension, data on the number and arrangement of pins of the IC,
in a further dimension, data on the meaning, the name and the signal flow direction of the pins of the IC,
in a further dimension, sequences of test instructions,
in a further dimension, test instruction headings which summarize individual test instructions,
in one dimension, specifies general test conditions,
in one dimension, specifies the start conditions for a test,
in one dimension, specifies test patterns,
in one dimension, specifies functional descriptions of the tests,
in one dimension, specifies switching values,
in one dimension, specifies conditions for quality sorting of ICs.

18. The method as claimed in claim 17, wherein the code generator (80) comprises at least one of the following components;
- a DC test generator which reads out and converts the data and control instructions from matrices, which generate DC voltage values for an IC in the test environment,
- an AC test generator which reads out and converts the data and control instructions from

matrices, which generate AC voltage values or signal curves for an IC in the test environment,

- a digital test generator which reads out and converts the data and control instructions from matrices, which generate digital voltage values for an IC in the test environment,

- a load board generator which reads out and converts the data and control instructions from matrices, which refer to the resources and requirements with respect to the load conditions of the load boards of the test environment,

- a test rule verifier which checks whether the data and control instructions of the syntax dependent on the test environment can be executed in the test environment,

and the code generator runs through a multistage method

- in the first stage of which the data and control instructions of a matrix are made available to the code generator as source information,

- in the second stage of which the source information is processed in succession, in each case by one of the components, the last component being the test rule verifier,

- and, in the third stage of which, the converted data and control instructions are modified by means of an optimizer with respect to resource utilization of a test environment, test speed, test sequences or waiting and idle times between individual data and control instructions.

19. The method as claimed in claim 18, wherein a

processible data sheet of the IC serves as the origin for the matrices independent of the test environment, on the basis of which data sheet automated test description documentations are generated from the matrices and name, in a generally legible manner, the scope, the type, the duration and the type of the data and control instructions.

20. The method as claimed in claim 19, wherein the individual specific test environments differ from one another in their structure and/or their syntax.

21. A data medium which can be processed by a microprocessor-controlled computer on which a method as claimed in claim 1 is physically incorporated.

22. A microprocessor-controlled computer having a central operating system which is electrically connected to at least one test environment on which a method as claimed in claim 1 runs.